A Vertical Junction Field Effect Power Transistor

Field of Invention

This invention relates to the creation and design of power semiconductor switches. More specifically, this invention relates to vertical junction field-effect power transistors with long vertical channels all having a highly uniform channel opening dimension defined and controlled by highly vertical p^+n junctions.

Background of the Invention

SiC power devices have been intensively investigated for the past 13 years. High power SiC vertical junction field effect-transistors (VJFETs) have attracted great attention for high temperature applications because VJFETs do not suffer from the low channel mobility problem of SiC MOSFETs. One SiC VJFET attempt, US patent No. 6,107,649 to J. H. Zhao entitled *Field-controlled high-power semiconductor devices* , the disclosure of which is hereby incorporated as reference, solves the problem of high electric field in the gate oxide of SiC MOSFETs by using lateral FETs to control the conduction of vertical channels without the need of epitaxial regrowth. Fig.1 is a copy of Fig.6A from US Patent No. 6,107,649. Another attempt, as found in the paper by K. Asano et al. entitled *5kV 4H-SiC SEJFET with low RonS of 69mΩcm²* published in IEEE ISPSD-2002, pp.61-64, cited herein as reference, has described a normally-off VJFET as shown in Fig.2 which also uses a lateral JFET to control a vertical channel but requires

expensive epitaxial regrowth at the middle of the device fabrication. The use of lateral JFET clearly results in higher device resistance leading to low current capability.

Purely vertical JFETs without the lateral JFETs have also been attempted but mostly in the forms of static induction transistors (SITs) which do not have long and highly uniform opening vertical channels defined and controlled by vertical pn junction gates. One attempt, as shown in Fig.3, Fig.4 and Fig.5 which are copies of Fig.5, Fig.3 and Fig. 10, respectively, from US patent No. 5,903,020 to R. R. Siergiej et. al. entitled *Silicon Carbide static induction transistor structure*, cited herein as reference, describes the formation of the p+ gates by normal incident, planar ion implantation on planar surface as shown herein in Fig.3, by normal incident, planar ion implantation onto shallowly etched surface as shown herein in Fig.4, and by normal incident, planar ion implantation onto only the deep trench bottoms as shown herein in Fig.5. These planar, normal incident ion implantation approaches do not result in long vertical channels with uniform channel opening dimensions as stated in US patent No. 5,903,020. Without highly uniform opening and long vertical channel, these SITs can not support high voltages. Besides they are difficult to be made normally-off switches capable of high voltage and high current. Fig. 6, a copy of Fig. 1 in the paper by J. Nishizawa et al. entitled *The 2.45 GHz 36 W CW Si recessed gate type SIT with high gain and high voltage operation* in IEEE Transactions on Electron Devices, Vol.4, No. 2, Feb. 2000, pp. 482-487, cited herein as reference, shows the well known silicon-based SIT design similarly without long vertical channels of a highly uniform channel opening dimension defined and controlled by p^+n junctions. One attempt has been reported to develop purely vertical JFETs with long

vertical channels up to 2um by Mega-eV ion implantation but without a highly uniform channel opening dimension, as shown in Fig.7 which is a copy of Fig. 1 in the paper by H. Onose, et al. entitled *2kV 4H-SiC junction FETs* published by Materials Science Forum, Vols.389-393, 2002, pp.1227-1230, cited herein as reference. The long vertical channel defined by Xj=2um shown herein as Fig.7 has a curved channel with a highly non-uniform vertical channel opening and a minimum opening dimension of Wch. In fact, SIT and VJFET gates formed by normal incident ion implantation generally lead to highly non-uniform channel opening dimensions similar to the curved channel of Fig.7. Although the channel is near 2um, the vertical part of the channel that has the same channel opening dimension is negligible in comparison to the total channel length. Hence, with a gate to source reverse bias as high as 50V to shut off the channel and create a large enough source-to-drain barrier, the vertical JFET blocks only 2kV, much below the theoretical blocking voltage limit of >3kV for the 20um thick structure shown in Fig.7 because of the absence of a long vertical channel with a highly uniform channel opening dimension. Besides, the device specific on-resistance is as high as $70m\Omega cm^2$. Furthermore, the vertical JFET is a normally-on switch, again due to the absence of long vertical channel with a highly uniform opening dimension defined and controlled to be normally-off by highly vertical p+n junctions. In fact, to the best of the inventor's knowledge, no normally-off VJFETs have been reported without using the present invention, although high power control systems clearly need normally-off switches to provide the important fail-safe protection. It would be clear to those skilled in the art that, to achieve a low device resistance in the conduction mode and to block high voltage in the blocking mode, a high voltage VJFET requires a large depth of the barrier between

the drain and source to prevent the well know drain-induced barrier lowering (DIBL) in FETs which leads to high leakage current and early breakdown of the switch. When the potential barrier along the source to drain direction is short in barrier depth as is the case for the vertical JFET shown in Fig.7 and SITs shown in Figs.3, 4, 5, and 6 as well as any other VJFETs and SITs with vertical channel defined by normal incident ion implantation gate, a large enough drain (blocking) voltage will pull down the barrier, causing electrons to flow from the source over the reduced barrier to the drain resulting in high leakage and early breakdown. Hence, up to date, all reported pure VJFETs and SITs without using present invention are normally-on and require a large negative gate voltage to over-pinch and shut off the channel so that a large enough source-to-drain barrier depth can be created for the devices to block high voltages. But gate-to-source pn junctions heavily doped on both sides tend to have a lower breakdown voltage and a larger leakage current under high reverse gate bias, not desirable for high power transistors.

Therefore, it is obvious to those skilled in the art that pure vertical JFETs with gate junctions formed by normal incident ion implantation without long vertical channels of a highly uniform channel opening dimension are not desirable for the implementation of normally-off operation. It is also obvious to those skilled in the art that pure vertical JFETs can not offer optimum normally-on operation when the gate junctions are formed by normal incident ion implantation without long vertical channels of a highly uniform channel opening dimension because an excessive negative gate bias is needed to create a barrier with enough depth to block desired voltages.

There is, therefore, a clear need to design a better performing SiC VJFET with long vertical channels all having a highly uniform channel opening dimension defined and controlled by highly vertical gate p^+n junctions so that higher power capability can be achieved with lower device resistance for either normally-off or normally-on operation.

Summary of the Invention

This invention provides new designs and implementations of pure vertical JFETs (VJFETs) ideally suited for realization in wide bandgap semiconductors such as SiC, GaN, diamond and the more traditional semiconductors such as silicon and GaAs as well as any other semiconductors suitable for high power and high frequency applications. The device includes a large number of paralleled cells fabricated on wafers with an n^+-n^--n-n^{++} structure, where the n^{++} is the top source layer for the source ohmic contact and for defining the boundary of the vertical p^+n junction gates remote from the top surface. The n^- layer forms the drift or blocking layer. The n layer is the channel layer used to form the vertical mesas and vertical channels. The n^- layer is for the blocking layer. The n^+ region is the bottom drain layer or substrate upon which the n^- blocking layer, the n channel layer n and the n^{++} source layer are grown. Each cell contains a highly vertical mesa defined by deep U-shaped trenches in the semiconductor with the center region of each mesa forming the long vertical channel of the cell. On each of the four side walls of a mesa, a U-shaped gate p+n junction is formed by angled or titled ion implantation of acceptors whose energy controls the vertical channel opening dimension, resulting in a highly uniform vertical channel opening. Gate ohmic contacts are placed on the bottom of

the U-shaped trenches on p^{++} region selectively formed by ion implantation on the bottom of the U-shaped $p^{+}n$ junction. The trenches are planarized by a standard planarization technique such as spin-coating of polyimide. Source ohmic contacts are placed on the mesa surface of the n^{++} top source layer. Drain ohmic contact is formed on the n+ bottom surface of the bottom drain layer. The n^{-} blocking layer and the n channel layer can be combined into a single n layer when separate optimization of the blocking and channel layers are not required.

Brief Description of the Drawings

Fig.1 shows prior art in the design of SiCVJFETs with lateral JFETs.

Fig.2 shows prior art in the design of SiC VJFETs with lateral JFETs.

Fig.3 shows prior art in the design of SiC static induction transistors (SITs).

Fig.4 shows prior art in another design of SiC static induction transistors (SITs).

Fig.5 shows prior art in yet another design of SiC static induction transistors (SITs).

Fig.6 shows prior art in the design of Si SITs.

Fig.7 shows prior art in the design of high voltage SiC VJFETs with long vertical channels.

Fig.8 shows cross sectional view embodying one form of the invention.

Fig.9 shows cross sectional view of formation of a long vertical channel with a highly uniform channel opening dimension by titled ion implantation of acceptors using thick and heavily doped n^{++} source layer by a self-aligned process.

Fig.10 shows cross sectional view embodying another form of the invention.

Fig.11 shows the cross sectional view of a 4H-SiC VJFET designed and fabricated according to the invention using a single $7x10^{15}cm^{-3}$ doped n-type layer for the drift layer as well as the vertical channel n layer.

Fig.12 shows the experimental room temperature I-V curves for the fabricated 4H-SiC VJFET.

Fig.13 shows the cross sectional view of a design for a 14kV SiC VJFET.

Fig.14 shows the simulated I-V curves for the 14kV SiC VJFET designed.

Detailed Description of the Preferred Embodiments

Now referring to Fig.8 with one embodiment of the VJFET where a four-layer semiconductor structure having top surface **155** and bottom surface **165** is used to fabricate the VJFET. The cross section of Fig.8 corresponds to a unit cell of the VJFET. A complete VJFET is formed by repeating this unit cell resulting in a large number of cells in parallel. The bottom drain layer **20** is a heavily doped n^+ bulk semiconductor upon which the epilayers are grown. On top of layer **20** is first grown a lightly doped thick n^- drift layer **40** followed by an n type channel layer **50**. For better layer quality, an epitaxial n+ buffer layer **30** can be used between layer **40** and substrate **20**. The thicknesses and doping concentrations for layers **40** and **50** are determined by the desired device voltage blocking capability and current requirement through well known device physics equations. Following layer **50** is an n^{++} layer **60** with a doping density higher than that of the p+ gate and with a thickness larger than the etch depth non-uniformity in photoresist (PR) and dielectric (such as polyimide) etch-back during a standard

semiconductor planarization process. The etch depth non-uniformity in semiconductor planarization process varies, depending on equipment used and processes employed, but is generally within the range of 0.2 to 2um although non-uniformity outside this range is also possible. Layer **60** can also be formed by ion implantation of donors, such as P or N either at room temperature or at high temperatures. The device includes the drain ohmic contact **150**; the vertical p+ gate **90** which, in this embodiment, is formed by first etching the deep U-shaped trench **75** (note: only half of the U-shaped trench is shown) to form the mesa **65** with highly vertical ($\beta \approx 90^{o}$) side walls, followed by tilted or angled acceptor ion implantation to the four sides of the mesa walls with a density lower than the donor density of the top source n^{++} layer **60**, which is typically 2 to $10x10^{18}cm^{-3}$ or higher, to form the highly vertical p+ gate **90** which defines a highly vertical channel **50** with a highly uniform channel opening dimension (d_0); the p+ trench bottom region **70** (or p+ body region **70**) typically doped in $10^{18}cm^{-3}$ range is formed by normal incident acceptor implantation; the p^{++} region of **80** which is for better ohmic contact and is formed together with region **70** but with increased acceptor dose near the surface region **95**; the metal ohmic contact **100** to the p^{++} region of **80**, which is internally connected to the vertical p+ gate region **90**; the passivation region **110** which can be formed by thermal oxidation followed by PECVD SiO_2 and PECVD nitride; the metal ohmic contact **140** to the n^{++} source region **60**; the dielectric trench fill **120** which planarizes the whole device surface; and the source metal overlay **130** which connects all the sources of individual cells. The vertical depth of the trench and the vertical depth of the p+ body implantation (region **70**) together determine the length (L_{VC}) of the highly vertical part of the channel. The length of L_{VC} should be designed to provide a negligible effect of the

well know FET DIBL barrier lowering. It should be obvious to those skilled in the art that there is a trade-off in the blocking voltage and device resistance. A longer channel length L_{VC} results in a larger channel resistance but a larger source-to-drain barrier, leading to a lower leakage current and a higher blocking voltage while a shorter channel length L_{VC} results in a smaller channel resistance but a DIBL barrier lowering and a higher leakage current, leading to a lower blocking voltage. Simulation results show that L_{VC} of 2.1 um can be used to implement SiC VJFETs up to 14kV as will be described in the section on examples. It is obvious to those skilled in the art that a L_{VC} shorter than 2.1um can be used for lower voltage VJFETs. For SiC VJFETs of 1.7kV to 14kV, L_{VC} in the range of 1 to 2.1um can be used. For VJFETs of a few hundred volts to 1.7kV, L_{VC} in the range of 1.5 to 0.5um can be used. The exact optimum length of L_{VC} depends not only on the maximum blocking voltage but also on the maximum allowed leakage current between source and drain of the VJFET and the normally-off or normally-on mode of operation which are all governed by the well known semiconductor device equations. For the vertical gate p+ implantation, the desired tilted angle, the implantation energy and the dose of acceptors depend on the desired vertical channel opening dimension which is largely determined by the channel doping concentration and the gate p^+n junction built-in voltage. For normally-off VJFET design, the vertical channel opening should be completely depleted by the built-in voltages of the p^+n junctions on each side the vertical channel. Because of the excellent highly vertical mesas that can be formed by dry etching and the tilted implantation with implantation depth that can be accurately controlled by implantation energies, the vertical channel opening dimension can be controlled to very

high accuracy in the submicron range, only limited by the masks used to define the source mesas.

In order to experimentally achieve the highly vertical channel with a highly uniform opening dimension throughout the entire vertical channel region and the entire wafer, it is critically important to use a heavily doped thick n^{++} source layer **60,** thick enough so that (i) self-aligned (by using metal on mesa as implantation mask) and tilted or angled implantation can be used to create p+ vertical side walls without converting any part of the top source layer **60** from n-type to p-type (as illustrated by Fig.9 where the parts of the source layer **60** below the dashed lines are implanted by acceptors but maintain the n-type property and (ii) the whole device surface can be planarized without exposing the top edge of the vertical p+ gate region **90** so that it is possible to form the source contact **140** and the final metal overlay **130** connecting all the source regions without shorting the top edge of the vertical p^+ gate **90** and the source ohmic contact **140** and source metal overlay **130**. Vertical arrows in Fig.9 indicate the direction of p+ body normal incident ion implantation. Titled arrows in Fig.9 show the direction of tilted angle ion implantation for the creation of the vertical p+ gate regions. Without a proper design of a heavily doped n^{++} source region **60,** the part of the n-type source layer subjected to acceptor implantation can be converted to p-type after the tilted, angled implantation to the vertical side walls of the mesa, making it very difficult to define the source ohmic contact without causing a short-circuit between the source contact metal **140** and the p^+ gate region **90.** Similarly, without a thick enough n^{++} source layer **60,** even if the source layer is doped very heavily, it would also be very difficult to form the source contact **140**

and the subsequent metal overlay **130,** without causing short-circuit between the source metal and the top of the p^+ gate. This is why the n^{++} layer **60** should be thicker than the etch depth non-uniformity encountered in the photoresist (PR) and dielectric (such as polyimide) etch-back during a standard semiconductor planarization process. The etch depth non-uniformity in semiconductor planarization process varies, depending on equipment used and processes employed, but is generally within the range of 0.2 to 2um although non-uniformity outside this range is also possible. A thick enough n^{++} layer **60** would allow the use of self-aligned processes to define source ohmic metal contact **140** to the top of the mesa surface **150**, and to form a thick metal overlay **130** connecting all mesa tops without shorting the p^+ gate **90** and the n^{++} source **60**.

In the blocking mode, the VJFET of Fig.8 operates by applying a high blocking voltage to the drain with respect to the source. For a normally-off VJFET, the vertical channel is off when there is no gate-to-source bias. For normally-on VJFET design, a reverse bias across the gate-to-source p^+n^{++} junction needs to be applied to turn-off the vertical channel. When the vertical channel is completely depleted, the reverse biased p^+ **(70)**-n^- **(40)** junction blocks the drain to source voltage. As the drain-to-source reverse bias is increased, the depletion width around the vertical p+ gate regions on either sides of the vertical channel **50** expands and substantially shields the source **60**. The maximum blocking voltage is therefore determined largely by the reverse biased p^+- n^- structure formed by the p^+ body region **70** and the n^- blocking region **40**. For a normally-off VJFET, a forward bias across the gate and source p^+n^{++} junction drives the device into the conduction mode by reducing the depletion width and opening up the vertical channel

so that current conducts between the drain and source. The forward bias does not need to fully turn on the gate-to-source p^+n^+ diode and the forward current going through the gate can be negligible in comparison to drain to source current. For normally-on VJFETs, reducing the reverse bias across the gate-to-source pn junction would open up the vertical channel and lead to current conduction between the drain and source. For a better surge current handling capability, this unipolar VJFET can also be operated in hybrid mode with a small quantity of hole injection by simply increasing the gate-to-source forward bias. The device is turned off after removing the gate-to-source bias in the case of normally-off VJFETs and after increasing the reverse gate-to-source bias to shut off the vertical channel in the case of normally-on VJFETs.

Referring now to Fig.10 with another embodiment of the invention where a bipolar VJFET is disclosed. The difference between the embodiment of Fig.10 and the embodiment of Fig.8 is in the use of bottom drain layer and buffer layer with conductivity type opposite to that of the blocking layer in Fig.10. Specifically, the bottom drain layer **220** in the specific illustration of Fig.10 is a heavily doped p-type substrate. The buffer layer **230** shown in Fig.10 is also a heavily doped p-type layer. The use of a bipolar drain junction results in a bipolar-mode VJFET which has a highly vertical channel with a highly uniform channel opening. For blocking operations, the bipolar-VJFET is biased in the same way as a unipolar VJFET of Fig.8. The vertical channel is pinched off at zero (reverse) gate-to-source bias for normally-off (normally-on) VJFETs and the blocking voltage is supported by the reverse biased p^+ (**270**)-n^-(**240**) junction. To turn on the device, an appropriate gate bias is applied to open up the vertical

channel to allow current passing from the drain to the source. Because the drain-to-source is formed by a p^+-n^--n^{++} structure in this bipolar VJFET instead of the n^+-n^--n^{++} structure in the unipolar VJFET, conductivity modulation due to hole injection into the thick n-type lightly doped blocking layer **240** will substantially reduce the device specific on-resistance.

Fig.11 shows the cross sectional view of a VJFET designed and fabricated according to the invention using a single $7x10^{15}cm^{-3}$ doped n-type layer for the drift layer as well as the vertical channel n layer. The length of the vertical part of the channel is designed to be 2.1um and the channel opening dimension is highly uniform and is designed to be equal to 0.55um. The top n^{++} source contact layer is doped $1x10^{19}cm^{-3}$ with a large thickness of 1.6um so that self-aligned gate p+ implantation can be done to form the vertical channel with a highly uniform channel opening dimension. The blocking layer thickness defined as the thickness of the n layer between the p+ body and n+ substrate is 9.4um when 0.2um p+ implantation tail is considered. The highly vertical channel is formed by first etching a deep trench of 3.2um, followed by titled Al ion implantation onto all four sides of the mesas forming accurately controlled vertical channels of 2.1um in length and a highly uniform vertical channel opening dimension of 0.55um. The vertical channel length of 2.1um is the sum of 1.6um of the U-shaped trench depth and 0.5 um of the p+ gate implantation depth. For higher blocking voltages, blocking layer doping density should be decreased and its thickness should be increased as well understood by those skilled in the art. Fig.12 shows the experimental I-V curves for the fabricated VJFET measured at room temperature. Fig.11 and Fig.12 are copied from

Fig.1 and Fig.4, respectively, in the paper entitled *3.6 mΩcm^2 , 1,726V 4H-SiC normally-off trenched-and-implanted vertical JFETs* after J. H. Zhao et al. published by IEEE ISPSD-2003, pp.50-52 and cited herein as reference. It is seen that the VJFET is capable of a blocking voltage (V_{bl}) of 1,726V with a specific on-resistance (R_{sp}) of 3.6mΩcm^2 at a drain to source voltage of 3V and a gate-to-source bias of 5V, corresponding to a figure-of-merit of V_{bl}^2/R_{sp} equal to 827MW/cm^2 which is the highest for any type of normally-off or normally-on SiC unipolar or bipolar power switches reported to date. In comparison to the normally-on vertical JFET by Onose et al. with 70mΩcm^2 and 2kV, this normally-off *3.6 mΩcm^2 , 1,726V* VJFET reveals the drastic advantage of the use of long vertical channels all having a highly uniform channel opening dimension defined and controlled by highly vertical p^+n junctions of the present invention. Fig.13 shows the design of a 14kV SiC VJFET and Fig.14 shows the simulated I-V curves for the 14kV SiC VJFET designed with the same 2.1um vertical channel length of Fig.11, confirming that SiC VJFETs with up to 14kV blocking voltage can be realized without changing the vertical channel length. Fig.13 and Fig.14 are copied from Fig. 8 and Fig.9 in the paper by J. H. Zhao et al. published by IEEE ISPSD-2003, pp.50-52.

While the preferred embodiments and specific examples are described herein those skilled in the arts would appreciate the fact that other variations are possible based on the invention. For example, the vertical channels can be formed by epitaxial refilling of p+ SiC into the U-shaped trench regions to define the desired vertical channels with a highly uniform channel opening dimension. As another example, the conductivity type of each